AMENDMENTS TO THE SPECIFICATION

Please replace the Title paragraph beginning at page 1, line 7, with the following amended Title paragraph:

FLUID EJECTION DEVICE WITH ADDRESS GENERATOR

Please replace the paragraph beginning at page 1, line 10, with the following amended paragraph:

This application is related to Patent Application Serial No. ~~[Not Yet Assigned]~~10/827,030, Attorney Docket No. 200210152-1, entitled "Fluid Ejection Device," Patent Application Serial No. ~~[Not Yet Assigned]~~ 10/827,139, Attorney Docket No. 200209168[[8]]-1, entitled "Fluid Ejection Device," Patent Application Serial No. ~~[Not Yet Assigned]~~ 10/827,045, Attorney Docket No. 200311485-1, entitled "Device With Gates Configured In Loop Structures," Patent Application Serial No. ~~[Not Yet Assigned]~~ 10/827,142, Attorney Docket No. ~~200209559~~200309559-1, entitled "Fluid Ejection Device," and Patent Application Serial No. ~~[Not Yet Assigned]~~ 10/827,135, Attorney Docket No. ~~200209237~~200309237-1, entitled "Fluid Ejection Device With Identification Cells," each of which are assigned to the Assignee of this application and are filed on even date herewith, and each of which is fully incorporated by reference as if fully set forth herein.

Please replace the paragraph beginning at page 14, line 21, with the following amended paragraph:

Pre-charged firing cell 120 is an addressed firing cell if both address signals ~ADDRESS1 and ~ADDRESS2 are low and node capacitance 126 either discharges if data

signal ~DATA is high or remains charged if data signal ~DATA is low. Pre-charged firing cell 120 is not an addressed firing cell if at least one of the address signals ~ADDRESS1 and ~ADDRESS2 is high and node capacitance 126 discharges regardless of the data signal ~DATA voltage level. The first and second address transistors ~~136~~ 138 and ~~138~~ 140 comprise an address decoder, and data transistor 136 controls the voltage level on node capacitance 126 if pre-charged firing cell 120 is addressed.

Please replace the paragraph beginning at page 31, line 29, with the following amended paragraph:

The gates of address seven transistors 458a and 458b are electrically coupled to shift register output signal line 410g. The drain-source path of address six transistor 458a is electrically coupled on one side to address line 472b and on the other side to evaluation line 476g. The drain source path of address ~~six~~ seven transistor 458b is electrically coupled on one side to address line 472c and on the other side to evaluation line 476g. A high level shift register output signal SO7 on shift register output signal line 410g turns on address ~~six~~ seven transistors 458a and 458b as address evaluation transistor 440g is turned on by a high voltage level evaluation signal LEVAL. The address seven transistor 458a and address evaluation transistor 440g conduct to actively pull address line 472b to a low voltage level. The address seven transistor 458b and address evaluation transistor 440g conduct to actively pull address line 472c to a low voltage level.

Please replace the paragraph beginning at page 56, line 13, with the following amended paragraph:

The timing pulse 610 of timing signal T3 at 608 is provided to shift register 402 in second

pre-charge signal PRE2, to direction circuit 404 in fourth pre-charge signal PRE4 and to address line pre-charge transistors 438 and evaluation prevention transistor ~~422a~~ 442a in logic array 406. During timing pulse 610 in second pre-charge signal PRE2, all shift register output signals SO 630 charge to high voltage levels at 640. Also, during timing pulse 610 in fourth pre-charge signal PRE4, reverse direction signal DIRR 642 charges to a high voltage level at 644. In addition, timing pulse 610 charges all address signals 625 to high voltage levels at 646 and turns on evaluation prevention transistor ~~422a~~ 442a to pull logic evaluation signal LEVAL 648 to a low voltage level at 650.

Please replace the paragraph beginning at page 56, line 23, with the following amended paragraph:

Timing pulse 614 of timing signal T4 at 612 is provided to shift register 402 in second evaluation signal EVAL2, to direction circuit 404 in fourth evaluation signal EVAL4 and to evaluation prevention transistor ~~422b~~ 442b in logic array 406. The timing pulse 614 in second evaluation signal EVAL2 turns on second evaluation transistor 518 in each of the shift register cells 403a-403m. With the internal node signals SN 626 at high voltage levels having turned on internal node transistor 520 in each of the shift register cells 403a-403m, all shift register output signals SO 630 discharge to low voltage levels at 652. Also, timing pulse 614 in fourth evaluation signal EVAL4 turns on fourth evaluation transistor 562. A control pulse at 654 of control signal CSYNC 624 turns on control transistor 564. With fourth evaluation transistor 562 and control transistor 564 turned on, direction signal DIRR 642 is discharged to a low voltage level at 656. In addition, timing pulse 614 turns on evaluation prevention transistor 442b to hold logic evaluation signal LEVAL 648 at a low voltage level at 658. The low voltage level logic evaluation signal LEVAL 648 turns off address evaluation transistors 440.

Please replace the paragraph beginning at page 62, line 7, with the following amended paragraph:

The timing pulse 810 is provided to shift register 402 in second pre-charge signal PRE2, to direction circuit 404 in fourth pre-charge signal PRE4 and to address line pre-charge transistors 438 and evaluation prevention transistor ~~422a~~ 442a in logic array 406. During timing pulse 810, all shift register output signals SO 830 are charged to high voltage levels at 840. Also, during timing pulse 810, reverse direction signal DIRR 842 charges to a high voltage level at 844. In addition, timing pulse 810 maintains all address signals 825 at high voltage levels and turns on evaluation prevention transistor ~~422a~~ 442a to pull logic evaluation signal LEVAL 848 to a low voltage level at 850.

Please replace the paragraph beginning at page 62, line 16, with the following amended paragraph:

Timing pulse 814 is provided to shift register 402 in second evaluation signal EVAL2, to direction circuit 404 in fourth evaluation signal EVAL4 and to evaluation prevention transistor ~~422b~~ 442b in logic array 406. Timing pulse 814 turns on the second evaluation transistor 518 in each of the shift register cells 403a-403m. With internal node signals SN 826 at high voltage levels that turn on internal node transistor 520 in each of the shift register cells 403a-403m, all shift register output signals SO 830 discharge to low voltage levels at 852. Also, timing pulse 814 turns on fourth evaluation transistor 562 and control signal CSYNC 824 provides a low voltage to turn off control transistor 564. With control transistor 564 turned off, reverse direction signal DIRR 842 remains charged to a high voltage level. In addition, timing pulse 814 turns on evaluation prevention transistor 442b to hold logic evaluation signal LEVAL 848 at a low voltage level at 858. The low voltage level logic evaluation signal LEVAL 848 turns off address

evaluation transistors 440.

Please replace the paragraph beginning at page 66, line 10, with the following amended paragraph:

Timing pulse 958 turns on third evaluation transistor 556. A control pulse 960 in control signal CSYNC 824 turns on control transistor 558 and forward direction signal DIRF ~~842~~ 858 discharges to a low voltage level at 962.

Please replace the paragraph beginning at page 67, line 12, with the following amended paragraph:

The select line 1008a conducts select signal SEL1 to address generator 1000, in one embodiment is timing signal T3 timing signal T6. The select line 1008b conducts select signal SEL2 to address generator 1000, in one embodiment is timing signal ~~T3~~ T4 timing signal T1. The select line 1008c conducts select signal SEL3 to address generator 1000 in one embodiment is timing signal ~~T3~~ T5 timing signal T2. The select line 1008d conducts select signal SEL4 to address generator 1000, in one embodiment is timing signal ~~T3~~ T6 timing signal T3. The select line 1008e conducts select signal SEL5 to address generator 1000, in one embodiment is timing signal ~~T3~~ T1 timing signal T4, and the select line 1008f conducts select signal SEL6 to address generator 1000, in one embodiment is timing signal ~~T3~~ T2 timing signal T5.

Please replace the paragraph beginning at page 83, line 25, with the following amended paragraph:

The second pre-charge transistor 1246 receives pre-charge signal PRE2 through signal

line 1208a, and evaluation transistor 1248 receives an evaluation signal EVAL through evaluation signal line ~~1246~~1214. If evaluation signal EVAL is set to a low voltage level and pre-charge signal PRE2 is set to a high voltage level, evaluation transistor 1248 is turned off and latched address line 1212 charges to a high voltage level through pre-charge transistor 1246.

Please replace the paragraph beginning at page 100, line 7, with the following amended paragraph:

The forward logic circuit 1604 is similar to logic circuit 406 (shown in Figure 9). The forward logic circuit 1604 receives the single high voltage level signal as an input signal AI1-AI13 and provides the corresponding low voltage level address signals in address signals ~A1, ~A2, ... ~A7. In response to a high voltage level input signal AI1, forward logic circuit 1604 provides address one address signals ~A1 and ~A2 at low voltage levels. In response to a high voltage level input signal AI2, ~~first~~ forward logic circuit 1604 provides address two address signals ~A1 and ~A3 at low voltage levels, and so on through and including a high voltage level input signal AI13 and forward logic circuit 1604 providing address thirteen address signals ~A3 and ~A5 at low voltage levels.

Please replace the paragraph beginning at page 112, line 19, with the following amended paragraph:

Data lines 208a, 208c, 208e and 208g are routed between printhead die side 1700a and ink feed slot 1704 and between ink feed slots 1706 and 1708. Each of the data lines 208a, 208c, 208e and 208g that are routed between printhead die side 1700a and ink feed slot 1704 is electrically coupled to pre-charged firing cells 120 in two fire groups 1702a and 1702d. Each of the data lines 208a, 208c, 208e and 208g that are routed between ink feed slots 1706 and 1708 is electrically coupled to pre-charged firing cells 120 in four fire groups 1702b, 1702c, 1702e and

1702f. Data line 208a is electrically coupled to pre-charged firing cells 120 in data line group D1 at 1710 to provide data signal ~D1. Data line 208c is electrically coupled to pre-charged firing cells 120 in data line group D3 at 1714 to provide data signal ~D3. Data line 208e is electrically coupled to pre-charged firing cells 120 in data line group D5 at 1718 to provide data signal ~D5, and data line 208g is electrically coupled to pre-charged firing cells 120 in data line group D7 at 1722 to provide data signal ~D7. The data lines 208a, 208c, 208e and 208g receive data signals ~D1, ~D3, ~D5 and ~D7 and provide the data signals ~D1, ~D3, ~D5 and ~D7 to pre-charged firing cells 120 in each of the fire groups 1702a-1702f. In one embodiment, data lines 208a, 208c, 208e and 208g are not routed the entire length of ink feed slots 1704, 1706 and 1708. Instead, each of the data lines 208a, 208c, 208e and 208g is routed to its respective data line group from a bond pad located along the side of printhead die 1700 nearest the data line group in the fire groups 1702a-1702f. Data lines 208a and 208c are electrically coupled to a bond pad along side 1700c of printhead die 1700, and data lines 208e and ~~208f~~ 208g are electrically coupled to a bond pad along side 1700d of printhead die 1700.